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Star-C - A New Converter Topology

Alexander Holmström

Division of Industrial Electrical Engineering and Automation
Faculty of Engineering, Lund University

Lunds Tekniska Högskola

Masters Thesis

StarC - A new converter topology

Author: Alexander Holmström

Supervisors:
Prof. Hans Bängtsson
Martin West
Gabriel Domingues

Examiner:
Prof. Mats Alaküla

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Abstract

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by Alexander HOLMSTRÖM

Power electronics is today used almost everywhere. The development of power electronics hardware is fast, pushing the performance limits. Still the conventional two level converter is the most commonly used converter on the market.

The output voltage of the conventional two level converter is generated as pulses. The pulses are generated with semiconductor switches with short switching times to keep the switching losses at an acceptable level. The big voltage steps combined with the short switching times cause very high voltage derivatives. Such derivatives generates high amounts of electro magnetic-emissions that may cause EMC-problems.

In this thesis two alternatives, with lower harmonic content, are investigated: multilevel converters and the new StarC converter. Multilevel converters synthesises the output voltage with pulses, much like the two level converter, but the DC-voltage is divided into more than two levels which results in smaller voltage steps and thereby reduced harmonic content. The StarC converter synthesises the output voltage by charging output capacitors with high frequency current pulses generated with a resonance link. The output voltage from the StarC converter is close to sinusoidal with very low harmonic content.

The investigated converters are simulated and compared in terms of total harmonic distortion, efficiency, current ripple and cost. The simulated application is traction of a car, with a motor model provided by Volvo used in the simulations.

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Abbreviations

ICE	**I**nternal **C**ombustion **E**ngine
DC	**D**irect **C**urrent
AC	**A**lternating **C**urrent
EMC	**E**lectro**m**agnetic **C**ompatibility
PWM	**P**ulse **W**idth **M**odulation
SPWM	**S**inusoidal **P**ulse **W**idth **M**odulation
MLC	**M**ulti**l**evel **C**onverter
NPCMLC	**N**eutral **P**oint **C**lamped **M**ulti**l**evel **C**onverter
CCMLC	**C**apacitor **C**lamped **M**ulti**l**evel **C**onverter
M2C	**M**odular **M**ultilevel **C**onverter
PMSM	**P**ermanently **M**agnetized **S**ynchronous **M**achine
FFT	**F**ast **F**ourier **T**ransform
THD	**T**otal **H**armonic **D**istortion
RMS	**R**oot **M**ean **S**quare

Symbols

V_{DC}	DC bus voltage	V
V_C	Capacitor voltage	V
E	Back electromotive force	V
i^{abc}	Three phase current vector	A
i^{dq}	Three phase current vector park-transformed	A
m	Number of voltage levels in the multilevel inverters	
m_a	Modulation index	
u_{ref}^{max}	Reference wave amplitude	V
u_{zs}	Zero-sequence voltage	V
C_r	Resonance capacitor	F
L_r	Resonance inductor	H
ω	Angular frequency	rads^{-1}
TX	Transistor X	
DX	Diode X	
R_s	Stator resistance	Ω
L_s	Stator inductance	H
Ψ_m	Magnetizing flux	Wb
T	Torque	Nm
p	number of poles	
$u_{rms,i}$	RMS voltage of i:th harmonic	V

Chapter 1

Introduction

1.1 Background

Over half of the industrial electrical energy is consumed by electrical motors [12]. Some examples are ski lifts, paper machines, pumps and fans for ventilation systems. In many cases these electrical machines run at constant speed, independent of the load. This is a very inefficient way of running the motor. By the use of variable speed drives the speed and torque of the motor can be controlled. This can increase the efficiency of the motor by running it at optimal operating points.

Today's most commonly used variable speed drive is the conventional 2-level converter. This converter synthesizes the output voltage by dividing the feeding DC-voltage into two voltage levels and switching between these two levels. Some advantages with the two-level converter is that it uses relatively few components and it is easy to control, but a major drawback is that the big voltage pulses generates high frequency electro-magnetic emissions that can cause unacceptable levels of electro-magnetic interference with other equipment in close proximity.

One way to improve the power quality and reduce the electro-magnetic emissions is to divide the voltage into more, smaller, voltage levels. This is the basic principle behind multilevel converters, where the DC-voltage is divided into three or more levels. With the increase in number of voltage levels the shape of the output voltage comes closer to the wanted sinusoidal waveform. The increase in number of voltage levels does however also increase the number of components needed and the complexity of the converter.

The Star-C is a new converter topology, invented by Hans Bängtsson at Bombardier. This converter improves the output power quality by synthesizing the output voltage by charging a capacitor with high frequency current pulses. The Star-C produces an output voltage close to perfect sinusoidal and looks like a strong contender to the conventional two-level converter for applications where emphasis is placed on output power quality.

This thesis work is done in cooperation with Volvo and Bombardier. The load used for testing the converters is an electrical prototype machine used in simulation work at Volvo. It is a 100kVA machine, and the intended application is traction of a car.

1.2 Purpose

The purpose of this thesis is to give an introduction to the Star-C converter and compare its performance with both the conventional 2-level and multilevel converters. The performance will be quantified in terms of cost, total harmonic distortion, efficiency and torque ripple.

1.3 Methodology

The first part of the thesis work consists of a literature study where the investigated topologies are presented. After that comes an evaluation for selection of topologies to investigate further. Lastly, simulations are done in order to verify and compare the selected topologies.

Chapter 2

Topologies

In this section the investigated converter topologies are introduced and the basic principle explained. The details of the modulation and component selection come later in chapters 4 and 5.

2.1 The Conventional 2-level Converter

The simplest DC to AC converter is the conventional two-level converter, see figure 2.1. It can supply a continues variable output voltage and frequency [1] even though it can only create two different output voltage levels, in each phase to the load, $V_{DC}/2$ and $-V_{DC}/2$. This is achieved by switching between those two levels fast with so called pulse width modulation (PWM), where the widths of the output pulses from the converter are adopted such that the mean value of the output voltage matches the voltage reference [3].

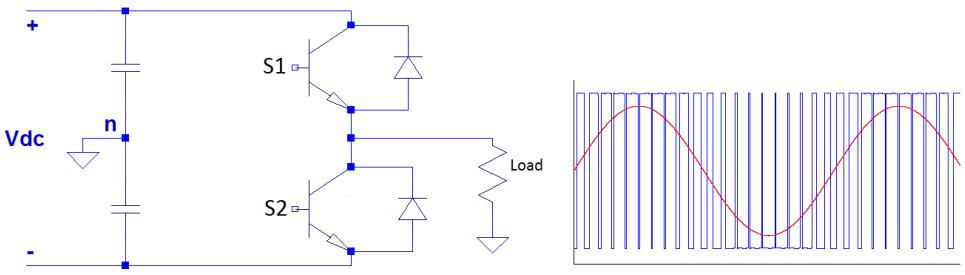

FIGURE 2.1: One phase leg of a 2-level converter and typical output voltage waveform.

PWM for the two-level converter is accomplished by comparing a reference wave, having desired output amplitude and frequency, with a triangular carrier wave. The carrier wave have an amplitude equal to half of the feeding DC voltage and the frequency depends on the application but have to be several times higher than the reference wave frequency [4]. The switch state change every time the reference crosses the carrier wave. The output from the converter is $V_{DC}/2$ when the reference is above the carrier and $-V_{DC}/2$ when the reference is below the carrier, see chapter 3.

The output pulses are generated with semiconductor switches. To keep switching losses low the switching time is short, typically 100ns [3], which when switching e.g. 600 V, gives dv/dt=600 kV/μs . As mentioned above these high voltage derivatives may cause EMC problems, which require some sort of physical implementation to reduce the electro-magnetic emission.

2.2 Multilevel Converters

The multilevel converters can produce more than two different phase potential levels. These kinds of converters can create smoother output waveforms with lower harmonic content than the conventional two-level converter [4]. This is achieved by dividing the DC voltage into several smaller voltage levels which, with unchanged switching time, reduces the voltage derivative (dv/dt). Another possibility with reduced voltage steps is to keep the dv/dt constant and reduce the switching time. This could also be very interesting, since modern transistors are getting shorter switching times to a point where shielding of cables and connectors are not enough to keep the electro magnetic emission down.

The basic principle of multilevel converters can be seen in 2.2. In a m-level converter, (m-1) capacitors are used to split up the DC-voltage into m levels. The voltage difference between each level becomes $\frac{V_{DC}}{m-1}$ and, by the use of switching, the desired voltage level is connected to the output.

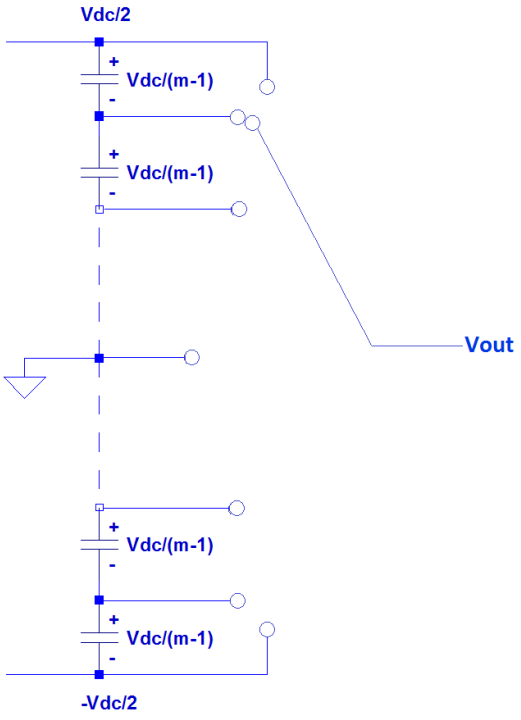

FIGURE 2.2: One phase leg of a simplified N-level converter.

The simplest multilevel converter is the three-level converter. It has a similar design to the conventional two-level converter, but it uses twice as many switches in each phase leg and so called clamping diodes connected to the neutral point between the capacitors clamping the voltage over each switch to one level [4], see figure 2.3. The three-level converter can create the three voltages $V_{DC}/2$, 0 and $-V_{DC}/2$ between the output and neutral point in each phase. To obtain e.g. $V_{DC}/2$ the two upper switches in figure are turned on which creates a connection between the load and the $V_{DC}/2$ point.

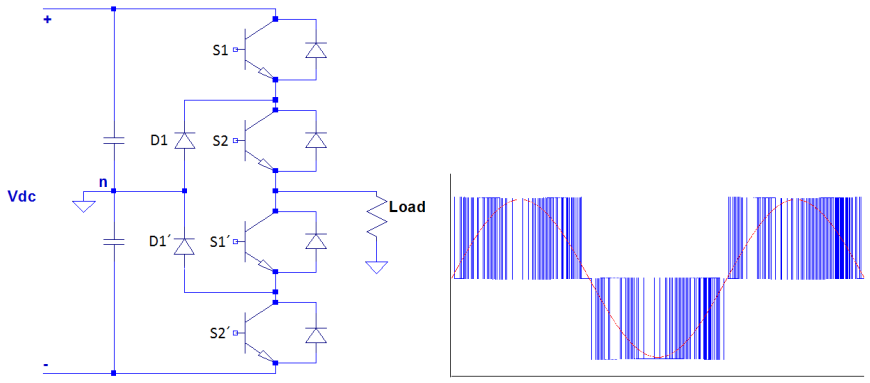

FIGURE 2.3: One phase leg of a 3-level converter and typical output voltage waveform.

The three-level converter mentioned above is a so called Neutral-Point Clamped Multilevel Converter (NPCMLC). There are several more MLC topologies, e.g. Capacitor Clamped MLC (CCMLC), Modular MLC (M2C), Cascade Multicell MLC and many more [4]. The multilevel converters investigated in this work are the NPCMLC, CCMLC and M2C.

2.2.1 The Neutral Point Clamped Multilevel Converter, NPCMLC

By adding more switches, DC-bus capacitors and clamping diodes the three-level converter mentioned above can be evolved into an converter with more than three voltage levels. These kinds of converters are called Neutral Point Clamped Multilevel Converters, but are also known as Diode Clamped Multilevel Converters. By series connection of several DC-bus capacitors the feeding voltage V_{DC} is divided into the voltage levels of the converter, (m-1) capacitors gives m voltage levels [4]. The number of DC-bus capacitors should be kept even in order to have the same amount of negative and positive levels. To be able to switch between the voltage levels, the converter needs m-1 switch pairs [5], see figure 2.4. With NPC converters it is possible to turn on and off every switch once per cycle and thereby generate a stepped sinusoidal wave with a fundamental frequency, and with low switching frequency comes low switching losses.

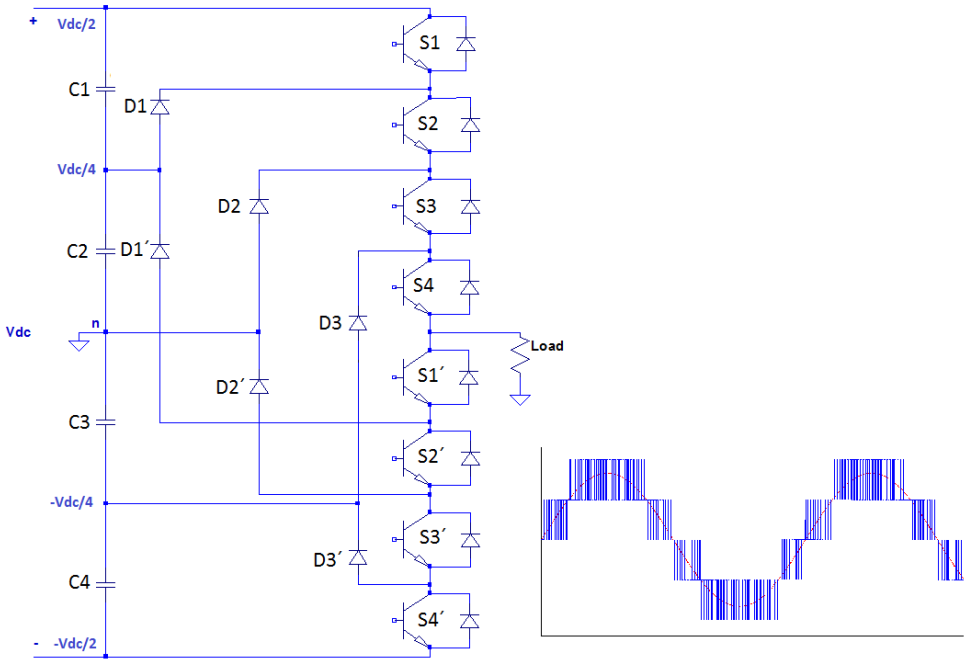

FIGURE 2.4: One phase leg of a 5-level neutral point clamped multilevel converter and typical output voltage waveform.

The clamping diodes are an essential part of the NPCMLC and help balancing out the voltage sharing between the switches [5]. This makes it so that every switch experiences a maximum voltage of $\frac{V_{DC}}{m-1}$. Note that some of the diodes experiences higher blocking voltages than the switches, e.g. D2 in figure 2.4 have to be able to block $\frac{V_{dc}}{2}$ when switches S1 and S2 are open. This can be solved by series connection of diodes, at the expense of higher cost and losses. With diodes with voltage rating equal to the switches, rated $\frac{V_{DC}}{m-1}$, the three level converter needs two clamping diodes see figure 2.2, the five level converter needs 12 clamping diodes see figure 2.4, and for a converter with m levels the number of clamping diodes needed is $(m-1)\times(m-2)$ [5]. The number of clamping diodes thus increases exponentially with the number of levels in the converter which makes it impractical to use the NPCMLI topology for converters with high amount of voltage levels. Note that if diodes with sufficient high voltage ratings are used there is no need for series connection and the number of clamping diodes would then be 2(m-2) [9].

A single phase five-level NPCMLC can be seen in figure 2.4. The five-level converter uses four DC-bus capacitors to divide the DC-bus voltage into the five voltage levels $V_{DC}/2$, $V_{DC}/4$, 0, $-V_{DC}/4$ and $-V_{DC}/2$, with the voltage $V_{DC}/4$ over each capacitor.

	Switch state							
Output	**S1**	**S2**	**S3**	**S4**	**S1′**	**S2′**	**S3′**	**S4′**
$\mathbf{V_{DC}/2}$	1	1	1	1	0	0	0	0
$\mathbf{V_{DC}/4}$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$\mathbf{-V_{DC}/4}$	0	0	0	1	1	1	1	0
$\mathbf{-V_{DC}/2}$	0	0	0	0	1	1	1	1

TABLE 2.1: Available switch states and corresponding output for the NPCMLI.

Each output and corresponding switching state for the 5-level NPCMLI can be seen in table 2.1. Note that the switches have unequal conduction duty for a sinusoidal output needing all voltage levels [6], e.g. switch S1 only conducts when the output is $V_{DC}/2$ but S4 is conducting for all outputs except $-V_{DC}/4$. This difference in current load means that the outer switches can have lower current ratings than the inner ones. Additionally the discharging time is different for each capacitor when transferring active power resulting in unbalanced voltages between the capacitors [6]. On the other hand

when the transferred power is only reactive, this unbalance problem does not occur since the charging and discharging time is the same for each capacitor [4], see figure 2.5.

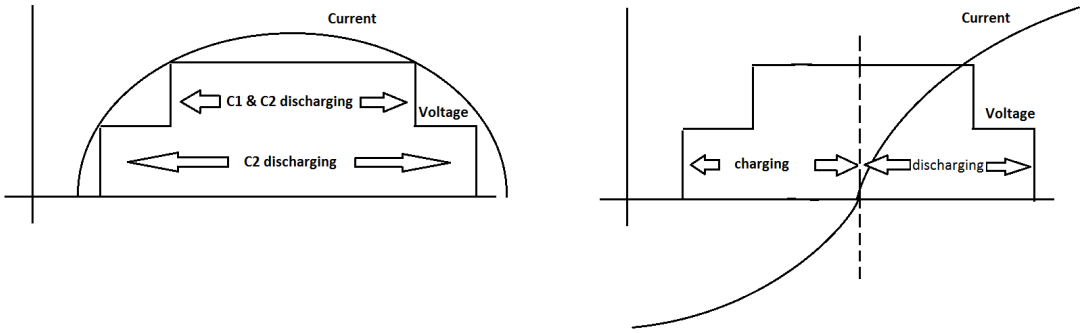

FIGURE 2.5: The left part of the figure shows active power transfer and the left part shows purely reactive power transfer. [4]

The single phase 5-level converter above can be extended to three phases by adding two identical switch legs with clamping diodes. The DC-bus with capacitors can be shared by all three phases.

2.2.2 The Capacitor Clamped Multilevel Converter, CCMLI

The Capacitor Clamped MLC, also called Flying Capacitor MLC, is very similar to the NPCMLC, see figure 2.6. The CCMLC got the same amount of DC-bus capacitors, m-1, and switch pairs, m-1 per phase, as the NPCMLC, but the clamping diodes are replaced with clamping capacitors. Unlike diodes the capacitors does not block reverse voltages which increases the number of available switch combinations, see table 2.3. An m-level CCMLC requires $\frac{(m-1)\times(m-2)}{2}$ clamping capacitors per phase, assuming the voltage rating of the capacitors is the same as that of the switches $(V_{DC}/(m-1))$ [6]. Note that if the voltage rating of the clamping capacitors is sufficient high there is no need of series connection.

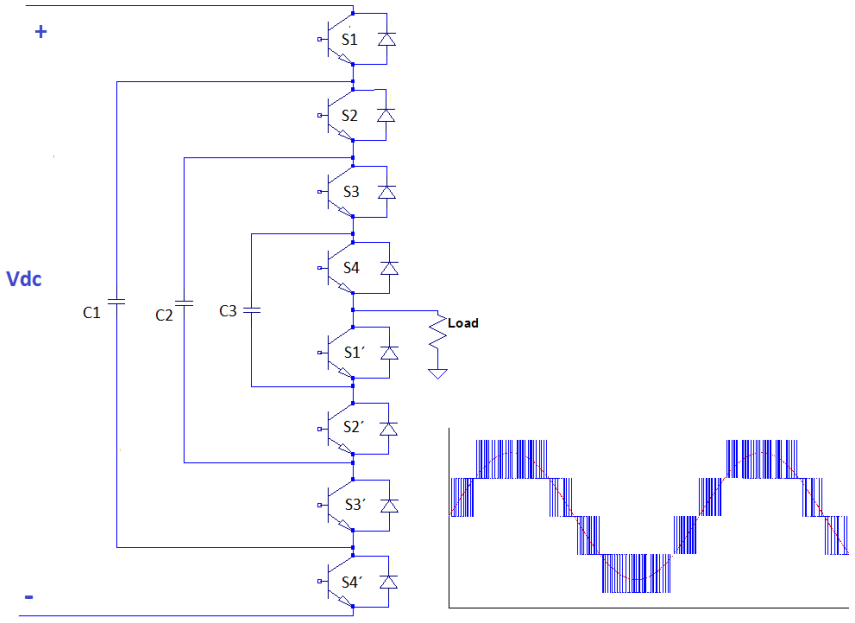

FIGURE 2.6: One phase leg of a 5-level capacitor clamped multilevel converter and typical output voltage waveform.

It is possible to choose switching states so that each switch only has to be switched once per cycle, making it possible to modulate with fundamental switching frequency. Table 2.2 lists a combination of switching states achieving this [6].

	Switch state							
Output	**S1**	**S2**	**S3**	**S4**	**S1′**	**S2′**	**S3′**	**S4′**
$\mathbf{V_{DC}/2}$	1	1	1	1	0	0	0	0
$\mathbf{V_{DC}/4}$	0	1	1	1	0	0	0	1
0	0	0	1	1	0	0	1	1
$\mathbf{-V_{DC}/4}$	0	0	1	0	1	0	1	1
$\mathbf{-V_{DC}/2}$	0	0	0	0	1	1	1	1

TABLE 2.2: Example of switch states that can be used at fundamental switching frequency.

The use of switching combinations shown in table 2.2 lead to unequal conduction duty for the switches, resulting in voltage unbalance between the capacitors when transferring active power, much like case for the NPCMLC (see figure 2.5). The voltage balancing problem can be addressed by using more of the possible switch states. Nevertheless, this requires a switching frequency higher than the fundamental. All the different switch

combinations that can be used to synthesize the output voltage can be seen in table 2.3 [5].

	Switch state							
Output	**S1**	**S2**	**S3**	**S4**	**S1′**	**S2′**	**S3′**	**S4′**
$\mathbf{V_{DC}/2}$	1	1	1	1	0	0	0	0
$\mathbf{V_{DC}/4}$	1	1	1	0	1	0	0	0
	0	1	1	1	0	0	0	1
	1	0	1	1	0	0	1	0
0	1	1	0	0	1	1	0	0
	0	0	1	1	0	0	1	1
	1	0	1	0	1	0	1	0
	1	0	0	1	0	1	1	0
	0	1	0	1	0	1	0	1
	0	1	1	0	1	0	0	1
$\mathbf{V_{DC}/4}$	1	0	0	0	1	1	1	0
	0	0	0	1	0	1	1	1
	0	0	1	0	1	0	1	1
$\mathbf{-V_{DC}/2}$	0	0	0	0	1	1	1	1

TABLE 2.3: Example of switch states that can be used at fundamental switching frequency.

Depending on what switch state is chosen, for a given output level, different capacitors are charged and discharged making it possible to keep their capacitor voltage levels balanced with the use of proper combinations [5]. However, this makes the selection of switch combinations complicated. Similar to the NPCMLC the single phase CCMLC in figure 2.6 can be extended to three phases by adding two more switch legs with shared DC-bus capacitors.

2.2.3 The Modular Multilevel Converter, M2I

The Modular Multilevel Converter (M2C) is a relatively new converter topology. It uses series connection of sub-modules to build up the output voltage levels [4]. The number of available output levels is proportional to the number of sub-modules in the converter. An M2C with m levels require $2 \times (m-1)$ sub-modules in each phase leg.

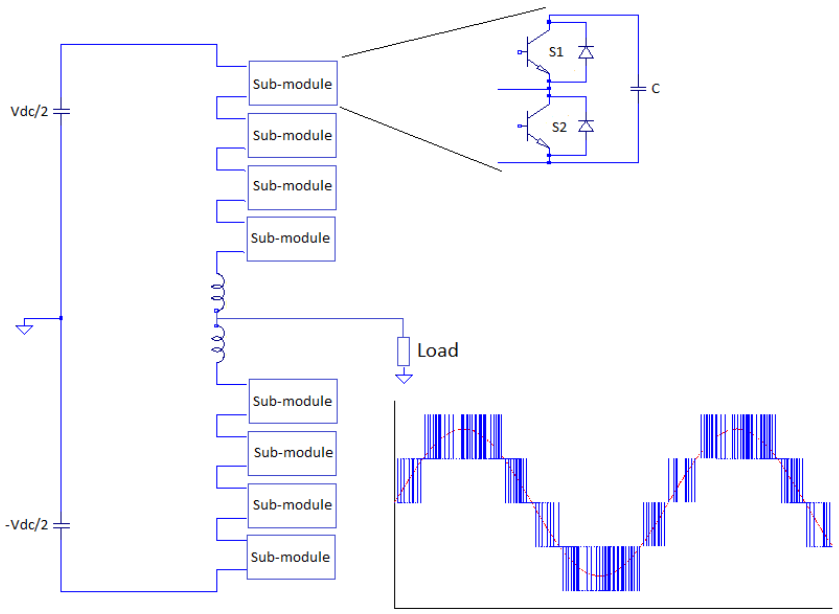

FIGURE 2.7: One phase leg of a 5-level Modular Multilevel Converter and typical output voltage waveform.

The inductors are there to make up for voltage difference between states [4]. Each sub-module consists of two switches, two diodes and a DC-capacitor charged to $\frac{V_{DC}}{m-1}$. The sub-modules can put out two voltages, $\frac{V_{DC}}{m-1}$ and 0 by connecting or bypassing the capacitor in the module. The output is thus created by the sum of the connected DC-capacitors [7]. To connect a certain sub-module and make its capacitor contribute to the output, switch S1 is switched on and S2 off, and to bypass the capacitor S1 is switched off and S2 on [4], see figure 2.7.

The current to the load flows through the connected modules and thereby changes the stored energy in the capacitors [7]. This means some kind of balancing modulation technique is needed in order to choose which capacitor to connect to keep the voltage between the capacitors balanced. Note that half of the submodules are connected and half of them bypassed at any given time to keep the sum of all connected modules equal to V_{DC} [4]. The capacitors in the submodules could be replaced with individual DC sources such as i.e. battery cells. This makes the M2C very interesting in the application with several DC-sources since it would not need any capacitors.

By adding two more phase legs, each with the same amount of submodules, the M2C in figure 2.7 can be extended to three phases.

2.3 The Star-C Converter

The Star C is a new converter topology proposed by Hans Bängtsson. This converter can provide a sinusoidal output voltage waveform by the means of charging output capacitors. This results in an output voltage with much lower harmonic content than the pulsed output voltage from conventional converters, see figure 2.8.

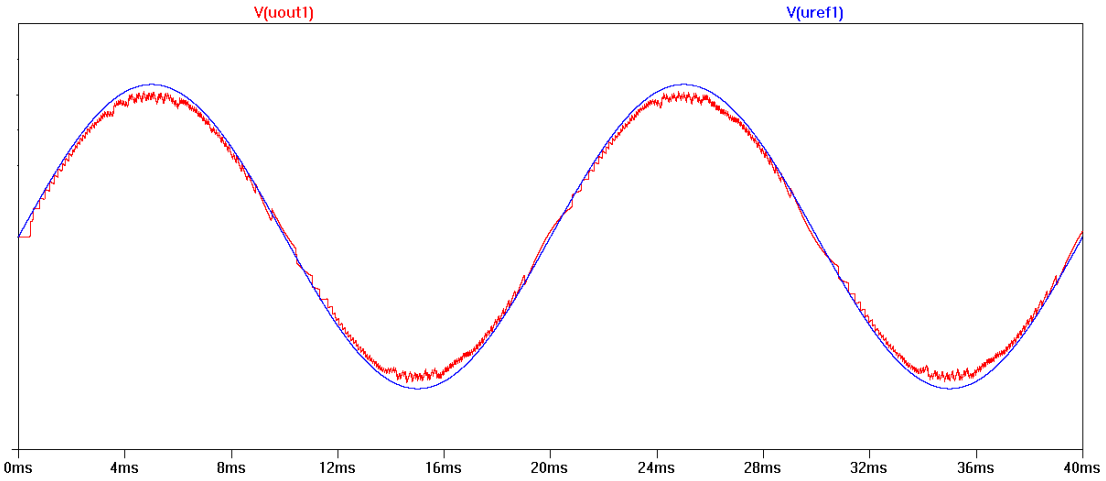

FIGURE 2.8: Typical output voltage waveform from the Star-C (red) and voltage reference (blue).

The function of the converter can be explained in three steps [3]:

1. The input stage is a four quadrant converter generating block shaped voltage pulses.
2. The current is then formed to semi sinusoidal pulses by an intermediate link.
3. The shaped current pulses are then fed to the right output phase, by the means of bidirectional switches, to charge the output capacitors.

The intermediate link, shaping the pulses, can either be realized as an series resonance link (see figure 2.9) or a inductive link by removing the resonance capacitor Cr. The principle for the two converters is the same, but the current pulses get different shapes depending on which intermediate link that is used.

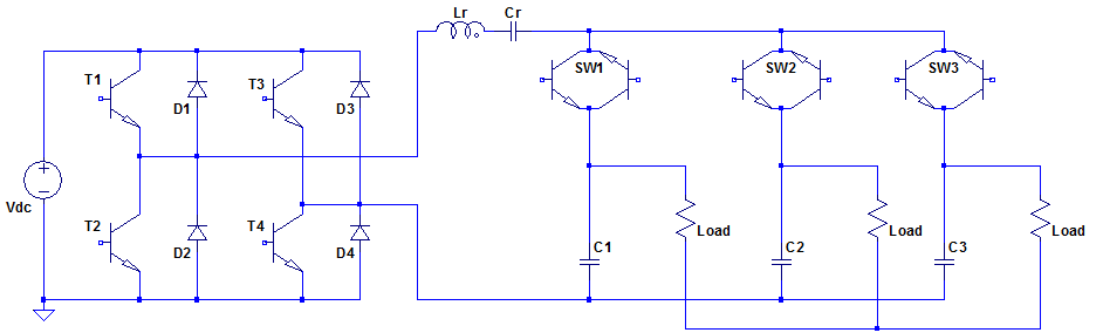

FIGURE 2.9: The series resonance version of Star-C. The bidirectional switches are represented with two transistors in different directions.

One drawback with the series resonance link is that it has to alternate the input pulses between negative and positive, which can cause problems when the load is unsymmetrical [8]. The advantage with the series resonance version, however, is that it is zero current switched. If the resonance capacitor is removed, the link becomes purely inductive, and by the means of hard switching the limitation of alternating pulses is removed. The drawback of the hard switched method is that the switching losses increase. In this thesis the load is assumed to be symmetrical and only the series resonance version of the Star-C converter is evaluated, henceforth, the Star-C converter refers only to the resonance version.

To generate a positive current pulse, to charge output capacitor C_1, the switches T_1, T_4 and the bidirectional switch SW_1 are turned on. The current starts to flow through the resonance link to the output capacitor C_1. During this time the resonance capacitor C_r is charged and the voltage drop over L_r decreases. This forces the current derivative to decrease and eventually become negative. At this point, the current starts to decrease. When the current reaches zero the switches T_1 and SW_1 are turned off. The same principle applies to negative current pulses, but involving T_2 and T_3 instead.

The output capacitors works like a filter with the function of transforming high frequency current pulses to a sinusoidal output voltage. The value of the output capacitor is tightly related to the output voltage ripple and THD. A larger capacitor gives less voltage ripple and thus lower THD, but it also increases the reactive current in the capacitor according to equation 2.1, where V is the output voltage amplitude and f is the output frequency.

$$I_C = V \times 2\pi f C \tag{2.1}$$

This means that the choice of the output capacitor is a trade-off between keeping the output THD low and the reactive current losses low. Increasing the output voltage frequency and amplitude also increases the reactive currents in the output capacitors.

A big advantage with the Star-C converter, compared with the two-level and multilevel converters, is that it can produce higher output voltages with the same DC-voltage on the input side. An example where this comes into play is applications where the requested output voltage got bigger amplitude than $\frac{V_{dc}}{2}$ (or $\frac{V_{dc}}{\sqrt{3}}$ if symmetrical references are used, see section 3.2). The 2-level and multilevel converters would then need a DC-DC boost converter, to increase V_{dc}, which could be skipped if a Star-C converter is used instead.

2.4 Topology Selection

The purpose of this section is to motivate the selection of which topologies to investigate further. As stated in previous section the most important criterion in the comparison between the different topologies is the cost. The cost of the converter is, obviously, tightly related to the number of components that is needed, however the rating of the components does also affect the cost.

The required component ratings for the different topologies can be seen in table 2.4. Note that the voltage rating of the components in the multilevel converters decrease with increased number of voltage levels, m, this is a big advantage with the multilevel converters. The current rating, however, is the same independent of the number of levels since each device has to be able to withstand the whole output current [4]. General expressions for voltage and current ratings for the Star-C is yet to be found. Component ratings needed for the Star-C, in the electrical machine application in this work, is discussed in chapter 4.

Topology	**2-lvl**	**NPCMLC**	**CCMLC**	**M2C**
VoltageRating	Vdc	$\frac{Vdc}{m-1}$	$\frac{Vdc}{m-1}$	$\frac{Vdc}{m-1}$
CurrentRating	I_{phase}	I_{phase}	I_{phase}	I_{phase}

TABLE 2.4: Ratings

The number of components needed for the different topologies can be seen in table 2.5, calculated with the assumption that they have the ratings in table 2.4. For the multilevel converters the component numbers are functions of available voltage levels, m.

Topology	**2-lvl**	**NPCMLI**	**CCMLI**	**M2I**	**Star-C**
Transistors	6	6(m-1)	6(m-1)	12(m-1)	10
Diodes	6	6(m-1)+3(m-1)(m-2)	6(m-1)	12(m-1)	10
Capacitors	2	(m-1)	$(m-1)+\frac{3(m-1)(m-2)}{2}$	2+6(m-1)	4
Inductors	0	0	0	6	1

TABLE 2.5: Number of components needed for the different topologies in a 3-phase setup with shared DC-bus.

Note that if the power source in the application consists of several DC-sources, i.e. battery cells, the M2C topology would not need any capacitors and thereby make it a very attractive option. In this thesis the power source is assumed to be a battery pack, so the M2C needs the number of capacitors stated in table 2.5.

The number of components needed for the multilevel converters increases fast with the number of voltage levels. For example, the jump from three to five levels, with the NPCMLC, requires additional 12 transistors, 42 diodes and 2 capacitors. Note also that every transistor switch needs its own gate driver. Even though the five level converter can use components with lower voltage ratings, they still needed to be able to withstand the same current.

With this in mind, only three level multilevel converters are studied further, to keep the number of components needed in the same range as the Star-C topology. The diode clamped converter (NPCMLC) is the best suited and most used three level topology. This is because of the self balancing property of the DC-bus capacitors and the fact that it does not need any pre-charged capacitors [9].

With the motivation above the three level NPCMLC is selected, from the multilevel converters, to be compared with the Star-C topology. The conventional two level converter is also investigated further and used as the reference topology.

Chapter 3

Modulation

3.1 SPWM - Sinusoidal Pulse Width Modulation

Sinusoidal pulse width modulation is the most common modulation technique used in the conventional two-level converter. In SPWM a sinusoidal reference wave, with desired output frequency, is compared to a triangular carrier wave [9]. When the instantaneous value of the sinusoidal wave is higher than the carrier the upper switch of the two-level converter is on and the lower switch is off resulting in the output $V_{DC}/2$. Else the lower switch is on and the upper off giving the output $-V_{DC}/2$, see figure 3.1.

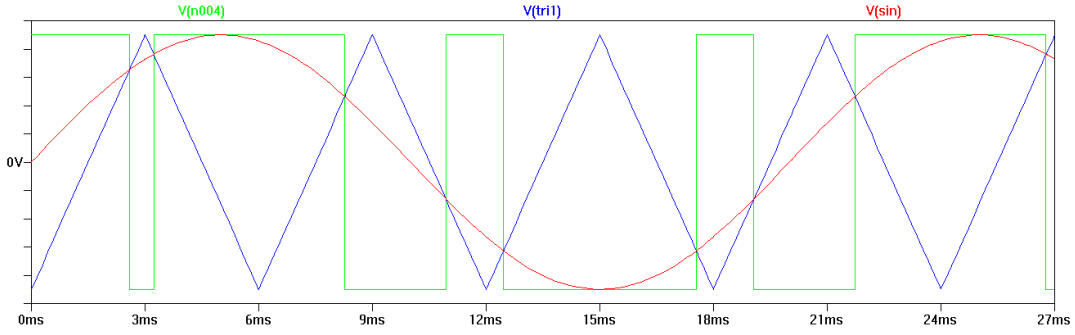

FIGURE 3.1: The red sine-wave is the reference, the blue triangular wave is the carrier and the green wave is the output voltage. (Note that the carrier frequency in the picture is very low for visualisation purpose.)

The triangular carrier wave has the amplitude of half the DC input voltage and the frequency varies for different applications. The frequency of the carrier wave has to be

several times higher than the frequency of the sinusoidal reference wave though. The output quality can be improved by increasing the carrier frequency (switching frequency), however this gives increased switching losses.

3.2 PWM for Multilevel Converters

The SPWM technique used in the two-level converter can be extended for use in the multilevel converters. This is done by having multiple carrier waves, with the same phase and frequency, on top of each other, see figure 3.2. One carrier wave can be used to control two switches which means m-1 carrier waves are needed for an m-level converter [9]. The amplitude of the carrier waves should be set so that they together span over the whole DC-voltage.

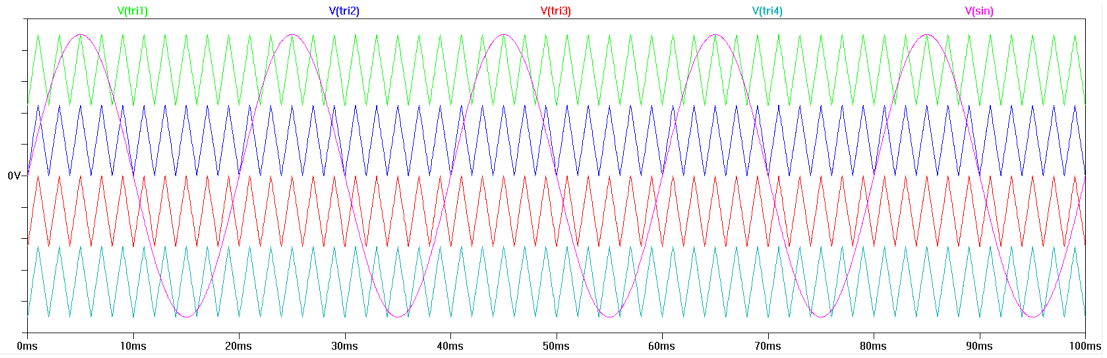

FIGURE 3.2: 5-level PWM example with 4 carrier waves (green, blue, red and cyan) and reference (purple).

Note that each switch experiences lower switching frequency than the frequency of the carrier wave. Take for example the green carrier wave in figure 3.2. This carrier wave controls two switches and when the carrier wave crosses the reference one switch is turned on and the other off. However, during most of the reference period there is no crossing between the green carrier wave and the reference, which means that one of the mentioned switches are on and one off during most of the time and only switched during the top part of the positive reference half-period.

With the use of sinusoidal references, the reference voltage amplitude must be kept below $V_{dc}/2$ to keep the modulation index below 1.

The modulation index m_a is defined as [10]:

$$m_a = \frac{u_{ref}^{max}}{u_{tri}} = \frac{u_{ref}^{max}}{V_{dc}/2} \tag{3.1}$$

where u_{ref}^{max} is the maximum amplitude of the reference wave and $u_{tri} = V_{dc}/2$ is the amplitude of the triangular wave. If m_a is higher than 1 over-modulation occurs, which means there is no crossing between the carrier and reference wave during some periods of the carrier wave. Over-modulation should be avoided since it limits the control of the converter and increases the harmonic content in the current [10].

As mentioned, if sinusoidal references are used, over-modulation occurs when the amplitude of the reference equals half the DC-link voltage. For better DC-bus utilization the zero-sequence voltage can be subtracted from the reference wave [9]. The zero-sequence voltage can be calculated from:

$$u_{zs} = \frac{1}{2}(max(u_{a,ref}, u_{b,ref}, u_{c,ref}) + min(u_{a,ref}, u_{b,ref}, u_{c,ref})) \tag{3.2}$$

The zero-sequence voltage is then subtracted from all the three references:

$u_{i,zs-ref} = u_{i,ref} - u_{zs}$

resulting in a higher maximal reference amplitude $u_{i,zs-ref}^{max} = V_{dc}/\sqrt{3}$. The new reference waveforms are called symmetrical reference waveforms [9], see figure 3.3.

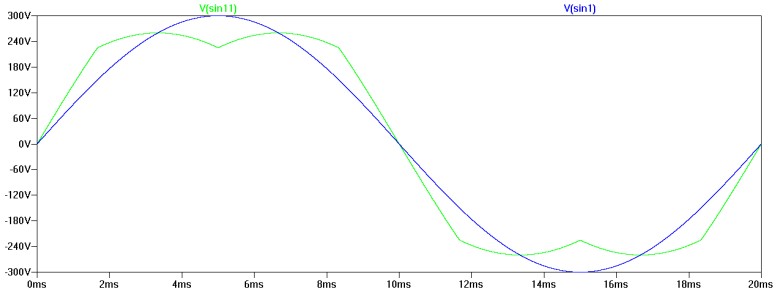

FIGURE 3.3: Sinusoidal (blue) and symmetrical (green) reference waveforms

3.3 Star-C Modulation

The modulator for the Star-C topology got 4 inputs: the voltage references from the current controller (one for each phase), the measured output voltages (one per phase), the direction of the next current pulse (negative or positive) and a voltage hysteresis

band. The outputs of the modulator are the wanted switch states for the H-bridge and the bidirectional output switches.

When it is time to sample the output voltage is measured and compared to the reference in all three phases. If the the difference between the reference and the output exceeds the hysteresis band in one phase, and the direction of the next current pulse corresponds to the pulse requested, the modulator sends a current pulse to that phase. If none of the phases requests a current pulse that corresponds to the direction of the next pulse the modulator waits until one of the phases needs a pulse in the right direction. Lastly if more than one phase needs a current pulse, that corresponds to the next pulse direction, the phase with the largest voltage error is prioritized.

Additionally the modulator calculates the voltage change a pulse is expected to cause before sending it. If the current error is larger than half of the expected voltage step the pulse is sent. However, if the output voltage error is smaller than half the expected voltage step the pulse would actually increase the error. In that case the controller does not send a pulse and thereby reduce redundant switching.

The switching frequency in the Star-C converter is equal to half the sampling frequency (in fact a little less than half the sampling frequency since sometimes none of the phases needs a current pulse). When a sample is taken, and there is a phase in need of a current pulse with the right direction, a current pulse is created. Only two switches are involved in creating a current pulse. For a positive current pulse, when delivering power from the DC-side to the AC-side (motoring mode), switches T1 and T4 in figure 2.9 are used, and for a negative pulse T2 and T3. With this in mind, and the fact that the pulses are alternated between positive and negative, it takes two sample periods for all the switches to be used.

The switching is done differently when running the Star-C converter in regeneration mode, that is when delivering power from the AC-side to the DC-side. Take for example a negative current pulse. First the stored energy in the resonance capacitor has to be moved to the resonance inductor. This can be done by opening switch T2, which causes a current to free-wheel through T2 and diode D4. When the current reaches its maximum switch T2 is turned off, which forces the current to continue through D1, the DC-source and D4 and charge the DC-source, see figure 3.4. The switching of the bidirectional switches remains the same as in motoring mode.

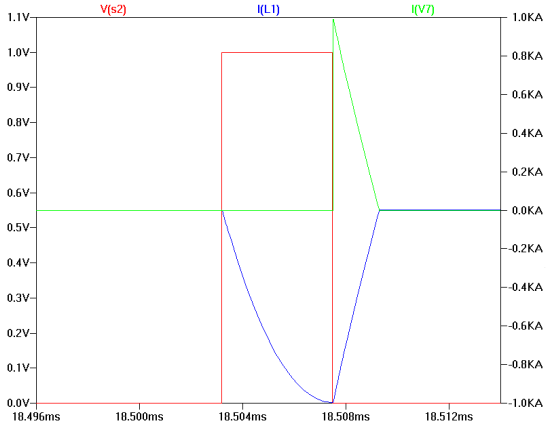

FIGURE 3.4: A negative current pulse (blue) in regeneration mode. The red waveform is the gate voltage on switch T2 and the green waveform is the current into to the DC-source.

A negative pulse in regeneration mode can also be achieved by the use of T3 instead of T1, and the modulator should alternate between the two to distribute the losses evenly. The same principle is used for positive pulses but involve T1 and T4 instead. Note that there is no longer zero current turn off of the switches in regeneration mode. In fact the switches have to turn off a very high current, which will cause high switching losses.

Unlike the conventional converter, the Star-C can only update one phase per sample. This means the Star-C has to sample three times as fast as the conventional converter to have the same effective update rate in the output voltage, this constitutes a drawback with the Star-C.

Chapter 4

Simulation Set-up

In this chapter the different system parts, the simulation set-points and converter simulation models are presented.

As discussed in section 2.4 the conventional two-level, the three-level and the Star-C topologies are selected for further investigation in simulations. The simulations are conducted in LTspice [8], a spice freeware from Linear Technology. The general setup for the simulations can be seen in figure 4.1.

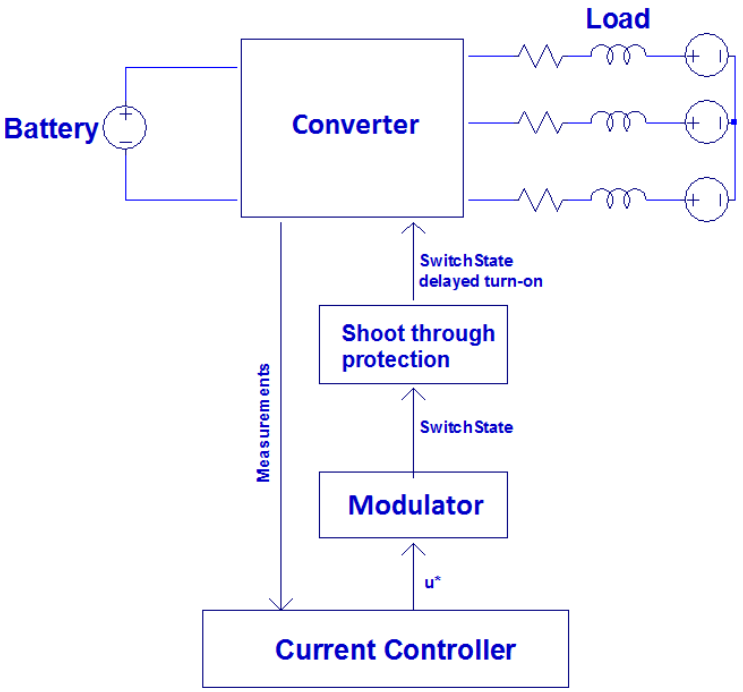

FIGURE 4.1: Simulation schematic overview.

4.1 System Parts

There are some system parts that are present in all the simulations, independent of the choice of converter. These parts are the battery, current controller, modulator, shoot through protection and load.

4.1.1 Battery

The battery is modelled with an ideal voltage source in the simulations. For the 2- and 3-level converter a voltage source of 600V has to be used to be able to run at the set-point discussed in section 4.2. The Star-C converter, however, does only need a 250V DC-source.

Note that the amplitude of the current pulses in the resonance tank of the Star-C increases with increased DC-voltage source, even though it runs at the same set-point. Increased current in the resonance tank increases losses and requirements on the resonance components. This means that the Star-C got best performance when the DC-source is chosen as small as possible, while still being able to follow the references.

4.1.2 Current Control and Load Model

The main task of an electrical machine is to produce torque. The torque of an electrical machine is proportional to the current flowing through the machine [10]. It is thus important to be able to control the current delivered from the converter to the machine.

To simplify calculations for the controller in a three-phase system a transformation from the three AC to two DC quantities is used. This transformation is called dq-transformation or Park transformation after Robert Park who first proposed it. The transformation refers the three-phase quantities to a reference frame fixed on the rotor, the dq-frame, resulting in the rotating variables being constant in this frame [11].

In the current controller the reference and measured currents, together with the feed-forward back emf, are transformed to the dq-frame where they are used to calculate the voltage needed to eliminate the current error. This voltage is then inverse transformed

back to three-phase system to be used as reference in the modulation. A block diagram describing the controller can be seen in figure 4.2

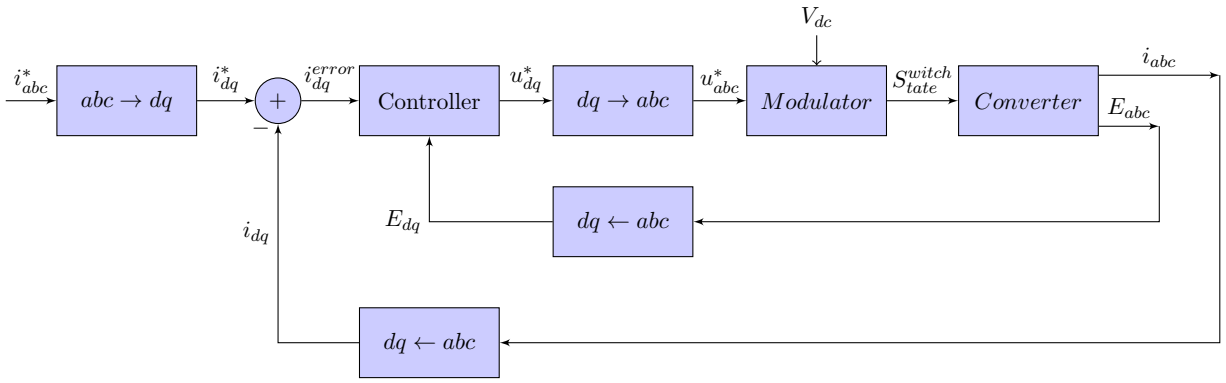

FIGURE 4.2: Block diagram describing the function of the current controller.

The load model used in this thesis can be seen in figure 4.3. It consists of a resistance (R), inductance (L) and back electromotive force (E). This is an idealized load, but the control methods used for this kind of load can easily be adapted to an electric machine [10].

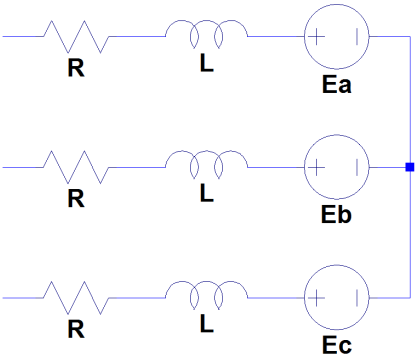

FIGURE 4.3: Generic 3-phase load

The voltage over the load can in dq-reference frame be expressed as equation 4.1 [10].

$$\vec{u} = R \times \vec{i} + L\frac{d\vec{i}}{dt} + j\omega L\vec{i} + \vec{E} \tag{4.1}$$

With a few assumptions, e.g. deadbeat control and that the back emf does not change much in one sampling period, the voltage equation 4.1 can be converted into a current control algorithm. The resulting controller equations can be seen in equation 4.2 and 4.3, for the full list of assumptions made and a complete derivation of the current control see [10].

$$u_d^*(k) = (\frac{L}{T_s}+\frac{R}{2})\times\left((i_d^*(k)-i_d(k)) + \frac{T_s}{\frac{L}{R}+\frac{T_s}{2}} \times \sum_{n=0}^{n=k-1}(i_d^*(n)-i_d(n))\right) - \omega L i_q(k) \quad (4.2)$$

$$u_q^*(k) = (\frac{L}{T_s}+\frac{R}{2})\times\left((i_q^*(k)-i_q(k)) + \frac{T_s}{\frac{L}{R}+\frac{T_s}{2}} \times \sum_{n=0}^{n=k-1}(i_q^*(n)-i_q(n))\right) + \omega L i_d(k) + E_q \quad (4.3)$$

Equation 4.2 and 4.3 gives the voltage reference in dq-coordinates, which are then transformed to three phase quantities to be used in the modulation. Additionally, the zero-sequence voltage is subtracted, as discussed in section 3.2, before the references are used in the modulation.

4.1.3 Modulator

The function of the modulator is to provide the converter with the correct switch states needed to make the output voltage follow the voltage reference provided by the current controller.

For the conventional 2-level converter the modulation is done by the use of normal pulse width modulation, see section 3.1. The 3-level NPC modulation is done in a similar way as the 2-level PWM, but uses two carrier waves instead of one, see section 3.2. The zero-sequence voltage is subtracted from the references from the current controller before compared with the carrier waves in both the 2- and 3-level versions. The switching frequency of the 2- and 3-level converters are chosen to 10kHz with two samples per switching period.

Note that the outer switches in the 3-level converter is only switched during half of the fundamental period and completely off during the other half period. The inner switches are also only switched during half of the fundamental period, while being completely on during the other half. This means that the switching frequency experienced by the switches in the 3-level converter is only 5kHz.

The modulation for the Star-C converter is done a slightly different way. The modulation principle is explained in section 3.3 and is implemented with sample-and-hold circuits and logical AND- and OR-gates. Since the Star-C converter can only update one phase

per sample it needs to switch three times as fast as the 2- and 3-level converter to have the same effective update frequency. With this in mind the switching frequency of the Star-C is chosen to 30kHz.

4.1.4 Shoot-Through Protection

Closing a switch is not instantaneous, which means it takes some time between the moment the switch gets the command to close and the moment the switch is actually closed. The same thing goes for opening the switch. The opening- and closing-time of the switch is typically 100ns [3], but the time for opening and closing is normally not exactly the same.

It is important that all switches in a phase leg are not conducting at the same time. This would cause a low resistant path between the power supply and ground, a so called shoot-through, resulting in a very high current that could damage the circuit. In all the converter topologies mentioned in this report one switch is turned off every time another is turned on. With this in mind shoot-through can be avoided by making sure the switch that is to be turned off is really off before the other switch is turned on.

Shoot-through protection is achieved by introducing a delay, a so called dead time, between the closing of one switch and the opening of another. This is implemented with the circuit in figure 4.4.

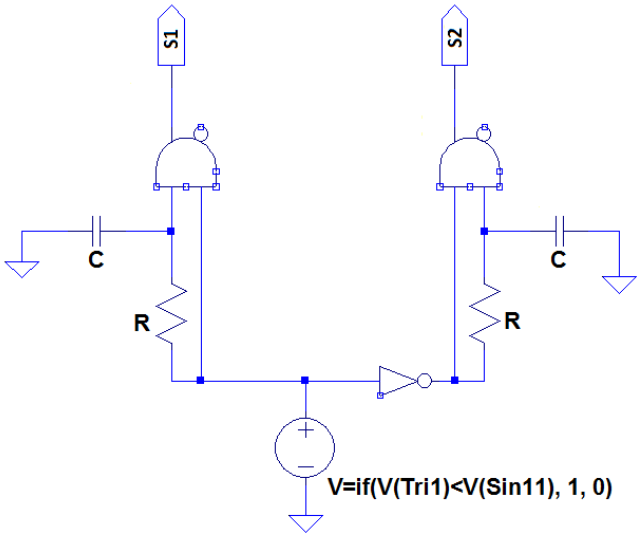

FIGURE 4.4: Control logic for the complimentary switches S1 and S2, with delayed turn on.

The behavioural voltage source at the bottom of figure 4.4 compares the voltage of the reference wave "Sin11" with the triangular wave "Tri1" and puts out 1V when the value of the reference is higher than the triangular wave, otherwise 0V. When the output of the behavioural voltage source is 1V the left capacitor starts to charge up through the left resistance. The voltage over the capacitor is then:

$$V_c = V(1 - e^{-t/RC}) \tag{4.4}$$

Since the AND-gate registers a logical 1 when the input is higher than 0.5V there is a delay between the moment the voltage source puts out 1V and the moment the output S1 is switched to 1V. When the output from the behavioural voltage source is 0V however, the S1 output will change to 0V instantaneously since there is a direct path between the voltage source and the AND-gate. The delay time can be determined by putting in $V_c = 0.5$ and $V = 1$ in equation 4.4:

$t = -RC \times ln(0.5) = RC \times 0.693$

By choosing R and C so that the delay time is higher than the turn-off time of the switches, shoot-through is avoided. The right leg of figure 4.4 works in the same way as

the left one with the exception that S2 puts out a delayed 1V when the output from the behavioural voltage source is 0V, otherwise an instantaneous 0V.

4.2 The electrical machine

The parameters for the load used in the simulations are taken from a permanently magnetized synchronous machine (PMSM) prototype-model used at Volvo. The parameters can be seen below.

$R_s = 0.0273\Omega$	Stator resistance
$L_{sd} = 0.738mH$	Stator inductance in d
$L_{sq} = L_{sd}$	Stator inductance in q
$p = 16$	Number of poles
$\Psi_m = 102.9mWb$	Flux linkage
$T_{mech}^{cont} = 250Nm$	Continues mechanical torque
$n_{mech}^{base} = 1335RPM$	Mechanical base-speed

TABLE 4.1: PMSM parameters.

The typical torque characteristics for an electrical machine can be seen in figure 4.5. The test-point used in the simulations is marked with a red circle in the figure. The simulations are thus performed at base speed, 1335RPM, and mechanical torque equal to 250Nm.

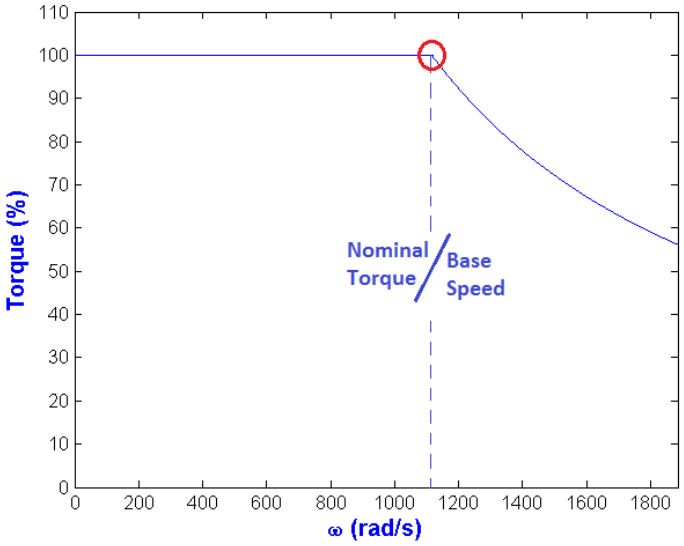

FIGURE 4.5: Torque characteristics.

The stator resistance and inductance are taken as value of R and L in the generic 3-phase load used in the simulations (see figure 4.3).

The base speed of the motor is n_{base}, at this mechanical speed the electrical frequency and angular frequency becomes:

$$\begin{aligned} \omega_{el} &= n_{base} \cdot \frac{2\pi}{60} \cdot \frac{p}{2} \\ f_{el} &= \frac{\omega_{el}}{2\pi} \end{aligned} \tag{4.5}$$

The torque is controlled by the means of quadrature stator current, meaning that the direct armature current is kept to zero ($i_{sd} = 0$). The reluctance torque in the machine is equal to zero since $L_{sd} = L_{sq}$. With this in mind, the torque equation simply becomes [10]:

$$T_{mech} = p/2 \cdot \Psi_m \cdot i_{sq} \tag{4.6}$$

For a given torque reference, T^*, the reference value for the current controller can be calculated as [10]:

$$i_{sd} = 0 \tag{4.7}$$

$$i_{sq} = (2/p) \cdot T^*/\Psi_m \tag{4.8}$$

Using the set-points for the current above the d- and q-component of the back-emf can be calculated from:

$$E_d = R_s \cdot i_{sd} - \omega_{el} L_{sq} \cdot i_{sq} \tag{4.9}$$

$$E_q = R_s \cdot i_{sq} + \omega_{el} \cdot \Psi_m \tag{4.10}$$

The values in table 4.1 together with equation 4.5 to 4.10 can now be used to find the parameters for the simulations:

$R_{load} = 0.0273\Omega$	load resistance
$L_{load} = 0.738mH$	load inductance
$f_{el} = 178Hz$	output frequency
$i_q = 303.69$	q-component of the current reference
$i_d = 0$	d-component of the current reference
$E_q = 115.08$	q-component of back emf
$E_d = -250.66$	d-component of back emf

TABLE 4.2: Parameters for the first simulation set-point.

Using the set-points in table 4.2 the power-factor becomes:

$p.f. = cos(atan(E_d/E_q)) = 0.417$

The low power-factor means that there is a lot of reactive current, generating additional losses in the converters, dragging down the efficiency. The reason for the low power-factor is the high inductance in the Volvo machine-model.

4.3 The Two-level converter simulation model

The simulation model for the 2-level converter can be seen in figure 4.6. The switches are modelled as one-directional switches with $2.7m\Omega$ on- and $10M\Omega$ off-resistance. In order to create some on/off switching time, a threshold voltage with hysteresis is implemented together with a capacitance on the gate. This switch model is also used in the simulations of the 3-level and Star-C converter.

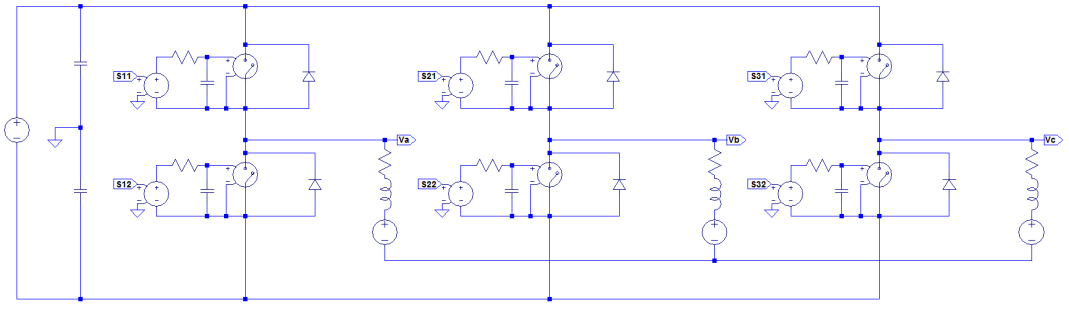

FIGURE 4.6: The simulation model for the 2-level converter with generic three phase load.

Since one switch is on and one off in each phase leg, at every time instance, the switches have to be able to withstand the whole DC-voltage of 600V. To leave some margin for e.g. voltage spikes a switch rated for 1200V should be used in a real implementation. The value of the DC-bank capacitors are chosen to 5mF.

4.4 The Three-level converter simulation model

The 3-level converter got two switches that are on and two that are off in each phase leg at any given time. By use of clamping diodes the DC-voltage is shared between the two switches that are off, see figure 4.7.

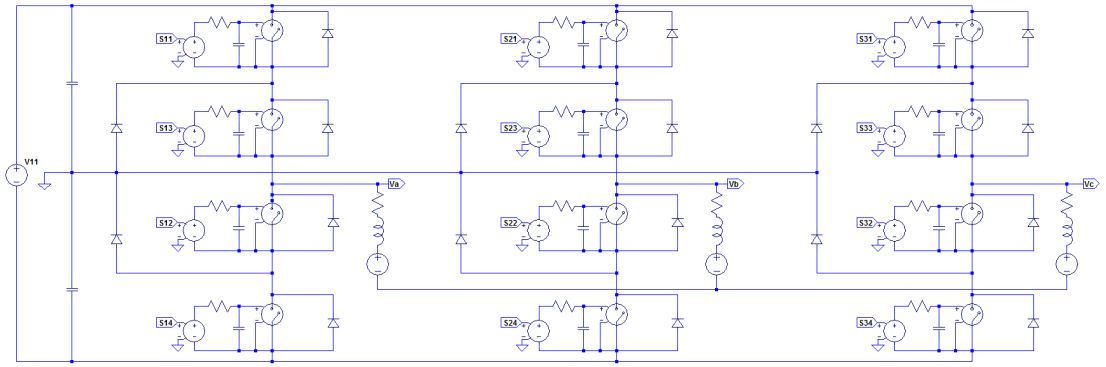

FIGURE 4.7: The simulation model for the 3-level converter with generic three phase load.

The voltage over each phase leg is shared between two switches in the 3-level converter, each switch must be able to block at least $\frac{V_{dc}}{2} = 300V$. Switches rated for 600V should be used in a real application.

As mentioned before, the three-level converter is self-balancing the DC-capacitors if the load is symmetrical. However, there are some small variations in the capacitor voltage, due to the current injected into the neutral point through the clamping diodes. The voltage variations are sinusoidal with frequency equal to three times the fundamental frequency, $178Hz \cdot 3 = 534Hz$. The DC-capacitors are chosen to 5mF, which gives the voltage variation in the capacitors an amplitude of 3.5V. This voltage variation is low enough to not make any significant impact on the harmonic spectrum of the output voltage.

4.5 The Star-C converter simulation model

The Star-C converter got a higher number of design parameters than the two- and three-level converters. For the Star-C the value of the output capacitor and the resonance capacitor and inductor must be decided, in addition to the switches.

First the value of the output capacitor is chosen, C_{out} in figure 4.8. A higher C_{out} gives less distortion in the output voltage but also increases cost, size and reactive current in the output capacitor.

The value of the resonance capacitor and inductor can be calculated from the relation in equation 4.11, where t_{td} is the deadtime and f_{sw} is the switching frequency in normal sense. Note that the load is not taken into account in the equation. However, the load does in fact affect the resonance frequency, which means that the values from equation 4.11 may have to be fine tuned to guarantee zero current switching.

$$L_r = \left(\frac{C_r \times C_{out}}{C_r + C_{out}} \times \left(\frac{\pi}{0.5/f_{sw} - t_{dt}} \right)^2 \right)^{-1} \tag{4.11}$$

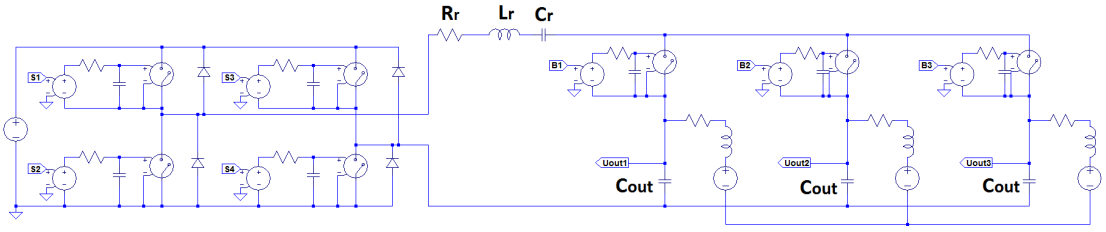

FIGURE 4.8: Star-C converter simulation model with generic three phase load.

The component values used in the simulations are $C_{out} = 1mF$, $C_r = 26.5\mu F$ and $L_r = 0.437\mu H$. A small resistance, R_r in figure 4.8, also has to be added in the simulation to limit the current pulses. The value of R_r is chosen to $100m\Omega$, and could possibly be skipped in a real implementation where the inductor windings actually got some resistance.

The switches in the H-bridge (see left part of figure 4.8) are the same onedirectional switches used in the 2- and 3-level converter simulations. Since one of the switches in

each leg of the H-bridge is on and one off at every time instance the switches in the H-bridge must be able to withstand the whole DC-voltage of 250V, which means H-bridge switches rated for 600V is sufficient for a real implementation.

Chapter 5

Results

In this chapter the simulation results are presented. All simulations are done with the electrical motor, discussed in previous chapter, running at base speed and maximum torque. The simulation models are presented in the previous chapter and the comparison and conclusions come in chapter 6.

5.1 Harmonic Distortion

THD is used to quantify the power quality of the converters. THD is the ratio between the rms voltage of the fundamental frequency and the sum of the rms voltages of all harmonics. It is defined as [9]:

$$THD(u) = \frac{\sqrt{\sum_{i=2}^{\infty}(u_{rms,i}^2)}}{u_{rms,1}} = \frac{\sqrt{u_{rms}^2 - u_{rms,1}^2}}{u_{rms,1}} \tag{5.1}$$

Where $u_{rms,i}$ is the i:th harmonic of the fundamental output frequency. $u_{rms,1}$, which is the rms voltage of the fundamental frequency, can be found in the FFT-plot of the output voltage. The output phase-to-phase voltage and FFT for the investigated converters can be seen in figure 5.1-5.3.

The Star-C converter offers some flexibility regarding THD versus losses. Increasing the allowed voltage ripple in the output, by increasing the voltage hysteresis band, reduces the number of current pulses. This reduces the current in all devices and thereby reduces

the losses, at the cost of a higher amount of harmonic content in the output voltage. The allowed voltage ripple is chosen to keep the THD below 5%.

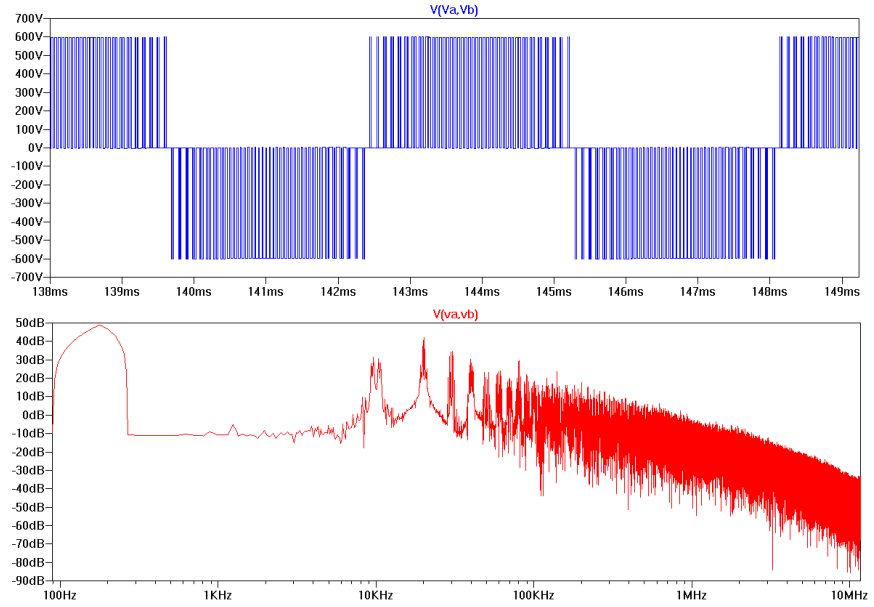

FIGURE 5.1: Output phase-to-phase voltage (blue) and its FFT (red) for the conventional 2-level converter.

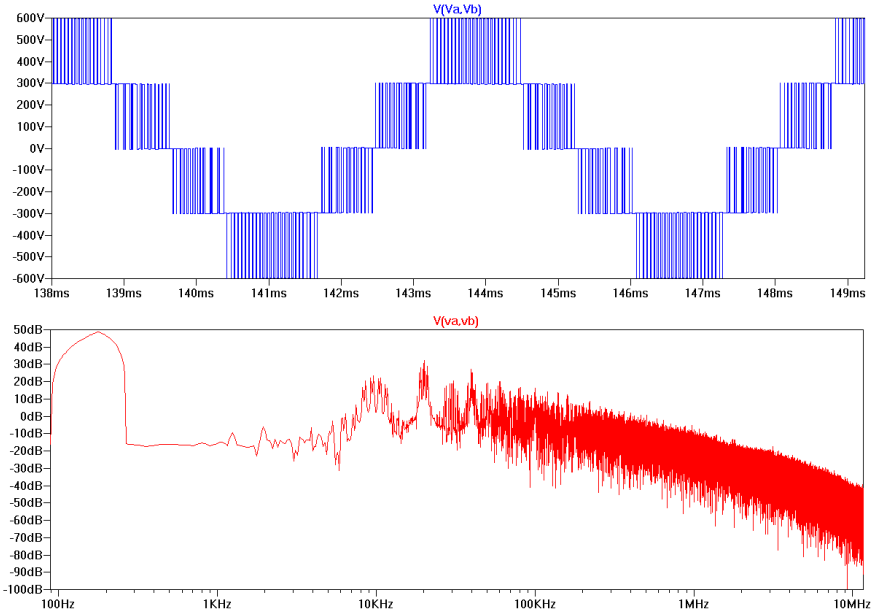

FIGURE 5.2: Output phase-to-phase voltage (blue) and its FFT (red) for the 3-level converter.

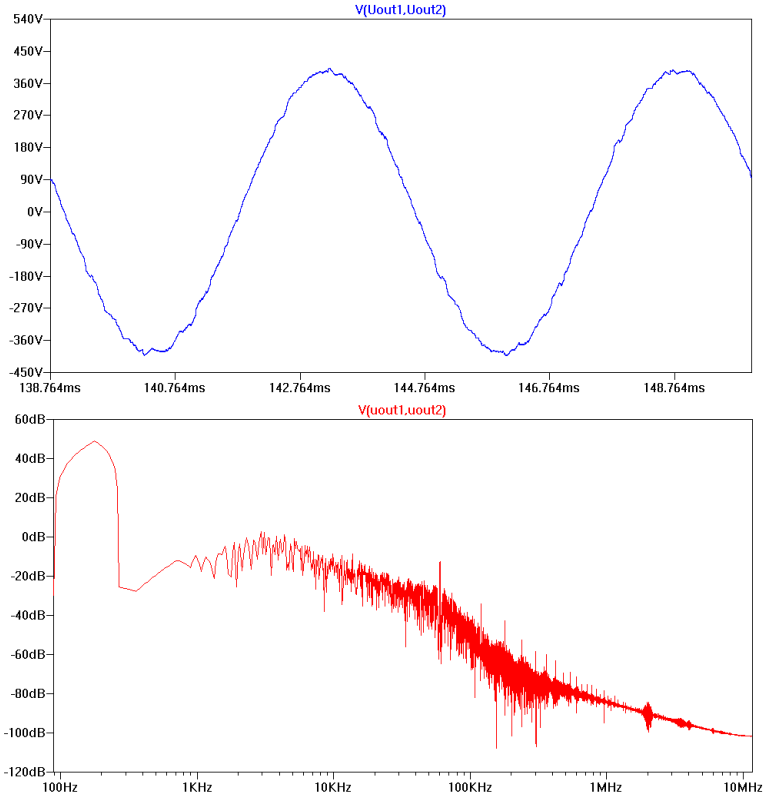

FIGURE 5.3: Output phase-to-phase voltage (blue) and its FFT (red) for the Star-C converter.

The results from the THD measurements can be seen in table 5.1.

	$u_{rms,1}$	u_{rms}	THD
2-level	279.692V	388.73V	96.5%
3-level	279.472V	304.27V	43.1%
Star-C	278.497V	278.74V	4.2%

TABLE 5.1

The two- and three-level converters got very similar frequency spectrum. The first spike is at the fundamental output frequency 178Hz. The switching frequency used in both cases is 10kHz. This shows up as a spike at 10kHz. The following spikes at 20kHz, 30kHz... are harmonics of the switching frequency. The three-level converter, however, got less of the very high frequency content compared to the 2-level converter. The switching frequency of 30kHz does not contribute to any considerable distortion in the Star-C converter, resulting in very low harmonic content.

5.2 Torque Ripple

A significant part of the torque ripple is caused by current ripple in the q-axis, see equation 4.6. Note that there are also other factors affecting the torque ripple, e.g. geometry of the rotor. In this work, however, only the q-current ripple is used to approximate the torque ripple. The q-part of the output current from the converters can be seen in figure 5.4-5.6.

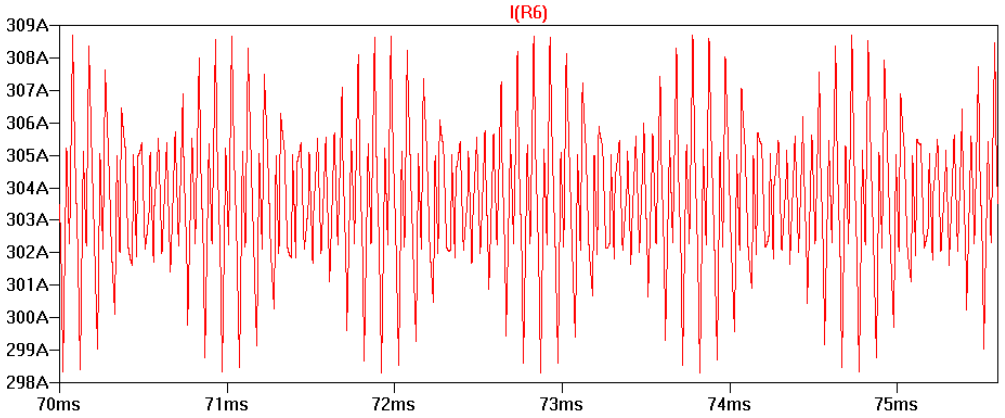

FIGURE 5.4: 2-level load current q-component.

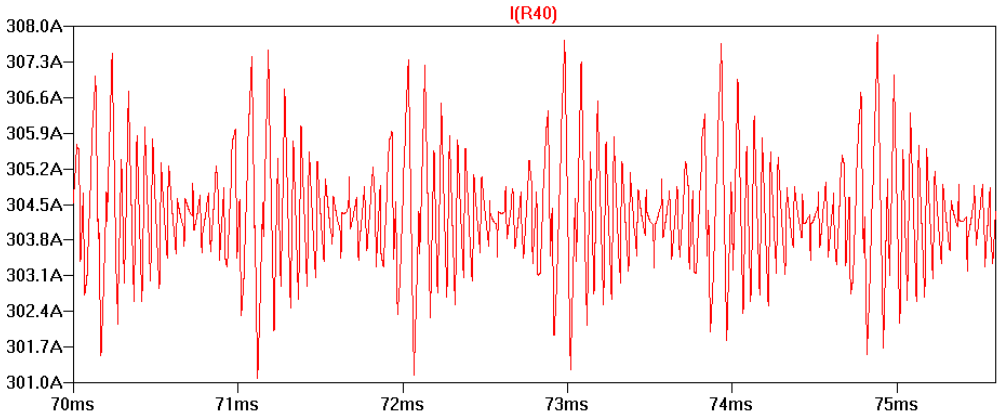

FIGURE 5.5: 3-level converter load current q-component.

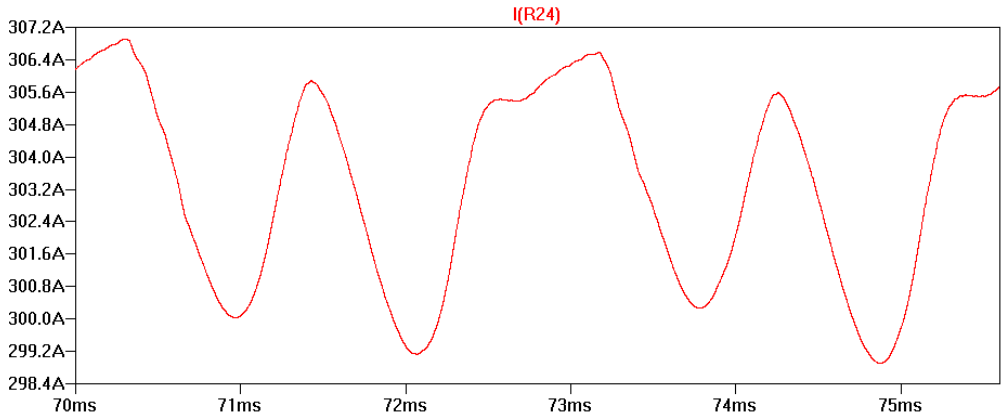

FIGURE 5.6: Star-C load current q-component.

The 2- and 3-level converters both have q-current ripple with at approximately 20kHz. The Star-C have significantly lower frequency ripple around 1kHz. The maximum peak-to-peak ripple becomes 10.3A for the 2-level, 6.4A for the 3-level and 6.7A for the Star-C converter. The maximum torque ripple, caused by the q-current, can be calculated by putting in these values into 4.6. This gives a torque ripple of 8.5Nm for the 2-level, 5.3Nm for the 3-level and 5.5Nm for the Star-C converter. Keep in mind that the output torque is 250Nm and compared to that all the converters have low ripple.

5.3 Power Losses

The power losses in the converters are mainly caused by the semiconductor devices in the 2- and 3-level converter. In the Star-C losses in the resonance inductor are also taken into consideration. The semiconductor losses are tightly related to the size of the semiconductors, and the size of the semiconductors depends on the current through and voltage rating of the device. The required area of the device depends on the heat losses it needs to be able dissipate, more losses means bigger area. A higher voltage rating means a thicker semiconductor, and a thicker semiconductor means more resistance and thereby also more losses. It is therefore desirable to chose the semiconductors with the lowest possible voltage rating to keep the efficiency of the converter high. The power losses does not only affect the efficiency of the converter but also the cost. This is because the power losses produces heat that has to be removed by the use of cooling. More losses means more heat, which in turn means a more expensive cooling system.

The losses in the semiconductor devices can be divided into conduction and switching losses. The conduction losses comes from the fact that there is an on-state resistance in the semiconductors that causes a voltage drop over the device when there is a current flowing through. The switching losses occur when the device transitions from conduction- to blocking-state or vice-versa.

The power loss estimation in this work is done by Gabriel Domingues. The estimations are based on the required voltage ratings of the devices and the current flowing through them, taken from the simulations. The power loss calculation can be done when the size of the semiconductor device is known. The sizing of the semiconductors is an iterative process. First a guess of the required size of the semiconductors are done. After that the power losses and heat dissipation can be calculated, based on the guessed size. If the size is to small the heat dissipation will be to low, and the process is restarted with a new larger size of the semiconductor, and if the semiconductor is oversized the process is restarted with a smaller size. By the use of this calculation process the optimal semiconductor size is found, and used for the power loss estimation.

When the voltage rating, V_r, and optimal semiconductor area, A, are found the losses can be calculated with:

$$P_{loss}^{igbt} = P_{cond}^{igbt} + P_{sw}^{igbt} = R_{CE}(A, V_r) \cdot I_{rms}^2 + V_{CE}(V_r) \cdot I_{ave} + f_{sw} \cdot [E_{on}(A, I_{ave}) + E_{off}(A, I_{ave})] \tag{5.2}$$

$$P_{loss}^{diode} = P_{cond}^{diode} + P_{rr}^{diode} = R_d(A, V_r) \cdot I_{rms}^2 + V_d(V_r) \cdot I_{ave} + f_{sw} \cdot E_{rr}(A, I_{ave}) \tag{5.3}$$

Where e.g. $R_d(A, V_r)$ means that the value of resistance R_d depends on the area and the voltage rating. The details of the dependency is not included in this report since Gabriel's work is not yet published.

The modulation technique used for generation in the Star-C converter is briefly explained in section 3.3. The big drawback with this method is that the transistors have to switch off a huge current, which would result in huge required area of the semiconductor and high losses. This would push up the cost of the Star-C converter to unreasonable levels. It is possible that the regeneration in the Star-C can be done in a different way, which would have softer requirements on the components. With this in mind only motoring-mode of the Star-C converter will be taken into consideration in the selection

of components for efficiency and cost calculations. For the 2- and 3-level converter both motoring and regeneration is used for the choice of components.

The efficiency of the converters, for both motoring- and generation mode, can be seen in table 5.2.

	2-level	3-level	Star-C
Motor	92.74%	92.19%	94.7%
Generator	91.85%	91.20%	Not calculated

TABLE 5.2

5.4 Cost

The cost calculations, based on the simulation data, are done by two PHD students at the department, Gabriel Domnigues and Pontus Fyhr. Gabriel's work takes care of sizing, choice of components and material cost while Pontus have cost models for production and packaging. The details of the cost calculations will not be included in this report since their work is not yet published. The hardware cost can be seen below in table 5.3, note that the hardware cost calculations are done under the assumption of big quantities ($\sim$ 10000 units).

	Power Modules	Drivers	Current Sensors	Voltage Sensors	Temp. Sensors	Control Unit	Cap.	Ind.	Miscellaneous Electronics	Total
2-level	2650	325	360	72	114	350	644	0	350	**4860**
3-level	2418	553	360	72	228	350	662	0	350	**4990**
Star-C	2344	489	600	288	190	350	11700	690	350	**17000**

TABLE 5.3: Hardware cost in Swedish Crowns

The hardware cost contains:

- Power modules with transistors and diodes.
- Gate drivers to open the switches.
- Current sensors, one per phase, for the current control.

- Voltage sensors, one in the DC-link for all converters and additionally one per phase for the Star-C.
- Temperature sensors, one per switch, for the cooling system.
- Control unit where the current control and modulator are implemented.
- Capacitors (DC-link-, resonance- and output-capacitors).
- Resonance inductor in the Star-C.
- Miscellaneous electronics refers to small additional components, for e.g. snubbers.

In addition to the hardware costs there are also costs related to production e.g. costs for connecting components and packaging. The estimated weight, box dimensions and production cost for the investigated converters can be seen below in table 5.4. Note that the cost is estimated under the assumption of a production of 10000 units, and that the cost per unit goes down with increased quantities and vice versa.

	Weight(kg)	Dimensions(m)	Production Cost(SEK)
2-level	9.8	0.48x0.50x0.22	**737**
3-level	9.2	0.43x0.50x0.22	**796**
Star-C	30	1.63x0.50x0.27	**2000**

TABLE 5.4: Weight, dimensions and production cost/unit.

Chapter 6

Conclusions

6.1 Discussion

This thesis gives a brief introduction to the new Star-C converter and compares it with the two level and multilevel converters. The intended application is traction of a small car. Several converters are investigated in theory, and from the investigated converters the two level, three level and Star-C are selected for further comparisons in simulations. The summary of the results can be seen in below in table 6.1.

	THD	ΔTorque	Efficiency (motoring)	Cost(hardware+production)
2-level	96.5%	3.4%	92.7%	5597kr
3-level	43.1%	2.12%	92.2%	5786kr
Star-C	4.2%	2.2%	94.7%	19000kr

TABLE 6.1: Result Summary

The step from two to three levels more than halves the harmonic distortion in the line-to-line voltage. The Star-C reduces the harmonic content even further. The output voltage from the Star-C has 10 times lower THD than that of the three level converter in the simulations. In terms of power quality the Star-C is uncontested when compared to the two- and three level converters. This makes the Star-C a very attractive option for applications with high requirements on the power quality. An example of this are applications where equipment in the close proximity is sensitive to electro-magnetic interference.

In this work the q-current ripple is used to approximate the torque ripple in the machine. The three level converter has less than half the amplitude of the torque ripple than the two level inverter, but with the similar frequency. The Star-C got similar ripple to that of the three level converter in terms of amplitude, but at a much lower frequency.

Surprisingly, the efficiency of the two- and three level converters are almost the same, even though the current in the three level converter passes through more semiconductor devices. The main reason for this is that the effective switching frequency of the devices in the three level converter is halved, see section 3.3. Additionally the three level converter can use switches with to two times lower voltage rating than the switches in the two level converter. This reduces the size of the semiconductor devices, and thereby also the resistance. The Star-C reaches even higher efficiency than the three level converter. This is because of the very low switching losses thanks to the zero current switching. However, this is only for motoring mode. When the Star-C is running in generation mode, with the hard switched method discussed in this work, it produces very high losses.

The manufacturing cost of the two- and three level inverter is almost the same, while the Star-C costs about four times as much. The reason that the three level converter can be as cheap as the two level one comes from the fact that smaller semiconductor devices with lower voltage rating can be used in the former. The main cause for the big price tag on the Star-C converter are the capacitors. The reason for the high capacitor cost are that several capacitors in parallel are needed to handle the high currents in the Star-C. This also makes the Star-C very big and bulky, compared to the two- and three level converters. Note, however, that filters are not considered in this work. There are applications where the two- and three level converter would need filters, that possibly could be skipped if the Star-C converter is used instead. This would atleast reduce the big price and size/weight difference between the Star-C converter and the other two.

It turns out that the hard-switched method used for generation in this work is not feasible. This implies that the Star-C is not very good for traction applications, since the generation of power when breaking is a very desirable attribute for traction. For other applications where only motoring mode is utilized, in e.g. fans and pumps, the Star-C could be a valid option.

This thesis barely scratches the surface of what is possible with the Star-C. There are a lot of applications, other than traction, where the Star-C could be better suited. It is also possible there are other ways, that are not considered in this work, to optimize the performance of the Star-C.

6.2 Future work

- Include filters in the comparison
- Lab prototype implementations
- One could argue that the big price difference between the Star-C and the three level converter motivates comparison with multilevel converters with higher amounts of voltage levels.
- Alternative method for regeneration in the Star-C

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